Enabling 8K displays

A story of 33M pixels, 2 CRTCs and no Tears!

MANASI NAVARE
Linux Graphics Kernel Developer
Open Source Graphics Center, Intel
XDC 2019 Montreal, Canada
8K BW vs. DP BW

33 M Pixels/ Frame

8K@60: 1980 M Pixels / Second

Total Display BW : 48 G Bits/sec

VESA DP

RBR/HBR for DP 1.1, 10.8 Gbps

HBR2 for DP 1.2, 21.6 Gbps

HBR3 DP 1.3/1.4, 32.4 Gbps
Can we stream 8K using single DP connector yet?

Required Display BW for 8K@60: >=48 Gbits/sec

Available BW of DP @ HBR3: 32.4 Gbits/sec

Output 8K using 2 DP connectors

Intel Icelake /Gen 11

Dell Ultrasharp 8K Monitor
Need for 2 CRTCs/Pipes on Intel HW

- Display BW should fit within Maximum Pipe Pixel Rate

- Max Pipe Pixel Rate = 2 * CDCLOCK
  - Max CDCLOCK on ICL = 652MHz
  - With 99% clock usability, max Pixel clock = \((2 \times 990 \times 652)/1000 = 1290\) MHz

- For 8K@60, Pixel Clock = 2200 MHz

  * Split 8K@60 across 2 CRTCs/ 2Pipes
Enable 8K in Dual Pipe Dual Port Configuration

8K Tiled Display
Parsed from Monitor’s DisplayID EDID data

Tile 1
3840 x 4320
DP link BW ~ 24Gb/s

Tile 2
3840 x 4320
DP link BW ~ 24Gb/s

Final 8K Display

DP 1 @ 32.4 Gbps
DP 2 @ 32.4 Gbps
Challenges with 2 CRTCs 2 PORTS

8K Frame Buffer

Pipe 1

Transcoder 1

Pipe 2

Transcoder 2

DP Port 1

Modeset on Pipe 1

Screen

Tearing

DP Port 2

Modeset on Pipe 2

Tile 1

Tile 2

Memory Interface

Scanout

Vblank1

DP1

Vblank2

DP2

Screen

Tearing
Solution: Transcoder Port Sync

△ PORT SYNC mode forces two or more transcoders involved in tiled modeset to be in sync

△ Only enabled in the slaves, HW lock-steps slave timings with the master
Last tile = master
Master crtc_state
Slave_bitmask = BIT(PipeA)

First tile = slave
Slave crtc_state
master_trans = PipeB

Enable Port Sync Mode
Set Master select

Output next frame
Atomic KMS changes

Userspace

Kernel

Dell 8K Monitor

DRM_IOCTL_MODE_GETCONNECTOR

Get Connector Tile Prop

Create FB, Setup CRTCs, Set CRTC offsets = Tile offsets

Intel_atomic_check Pipe A (Slave)
Master = B, slave_mask = 0

Intel_atomic_check Pipe B (Master)
Master NULL, slave_mask = BIT(PipeA)

Hot Plug Detect

Tile Info in Display ID/ Set Connector TILE Prop

Modeset in Master CRTCs commit()

Get slave_crtc_state
Slave CRTC enable, enable Port_sync, select master, enable slave TRANS
Slave Link train, DP_TP_CTL = Idle
Master CRTC enable
Master Link train, DP_TP_CTL = Idle
Set Slave DP_TP_CTL = Normal
Set Master DP_TP_CTL = Normal

Plane updates, Pipe register updates, Page flips for Master + Slave

Atomic Check

Atomic Commit
Synchronized page flips validation/CI

△ IGT test kms_dp_tiled_display.c and TILE property parser to decode the tile information added to igt/lib/igt_kms.c

△ Validate by capturing page flip event timestamps on each CRTC and ensuring they are within 10us (credits: Madhumitha, Simon Ser)
8K Results with PORT SYNC

△ Support for transcoder port sync and dual pipe dual port 8K tiled display to land in 5.4.0 Linux Kernel
Questions?

Thanks to the entire Intel-gfx and dri-devel community!!

Manasi.d.Navare@intel.com
IRC: mdnavare@intel-gfx, dri-devel on freenode
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